FIG. 1

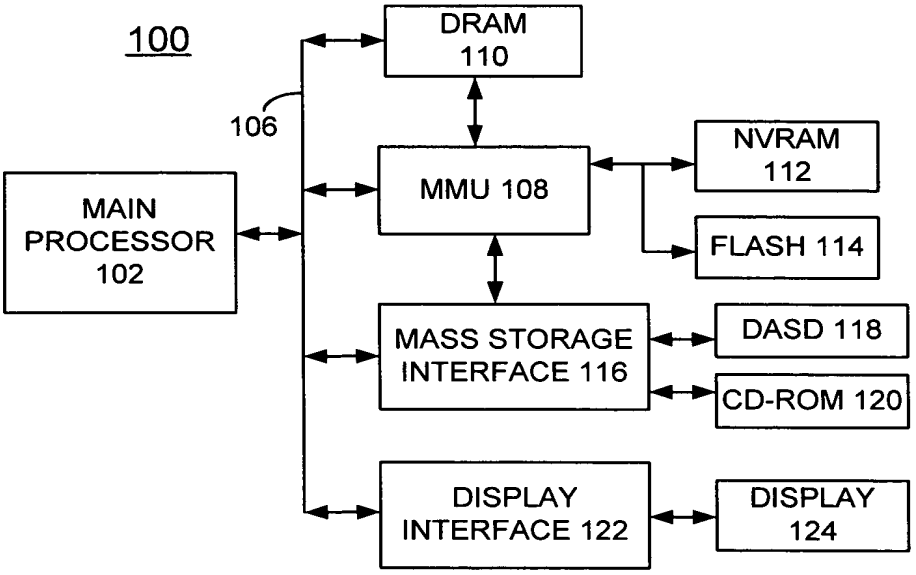
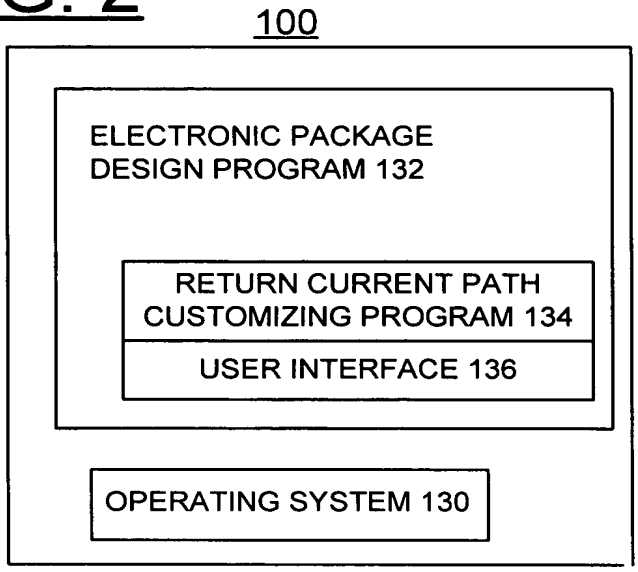

100
DRAM 110
106
NVRAM 112
MMU 108
MAIN PROCESSOR 102
FLASH 114
MASS STORAGE INTERFACE 116
DASD 118
CD-ROM 120
DISPLAY INTERFACE 122
DISPLAY 124

FIG. 2


100
ELECTRONIC PACKAGE DESIGN PROGRAM 132
RETURN CURRENT PATH CUSTOMIZING PROGRAM 134
USER INTERFACE 136
OPERATING SYSTEM 130

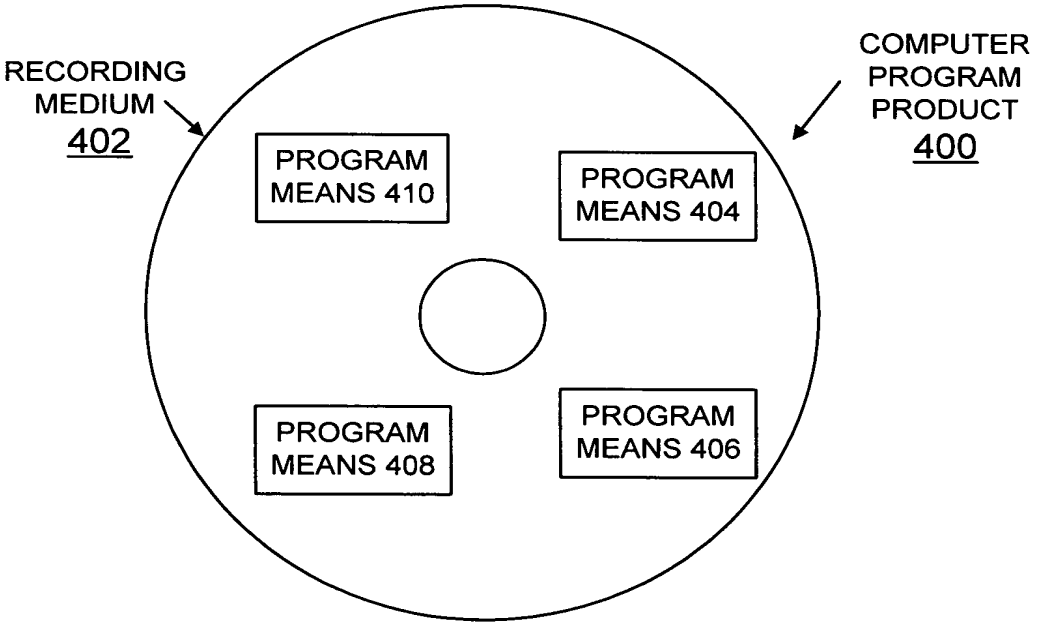

RECORDING MEDIUM 402
COMPUTER PROGRAM PRODUCT 400
PROGRAM MEANS 410
PROGRAM MEANS 404
PROGRAM MEANS 408
PROGRAM MEANS 406

FIG. 4

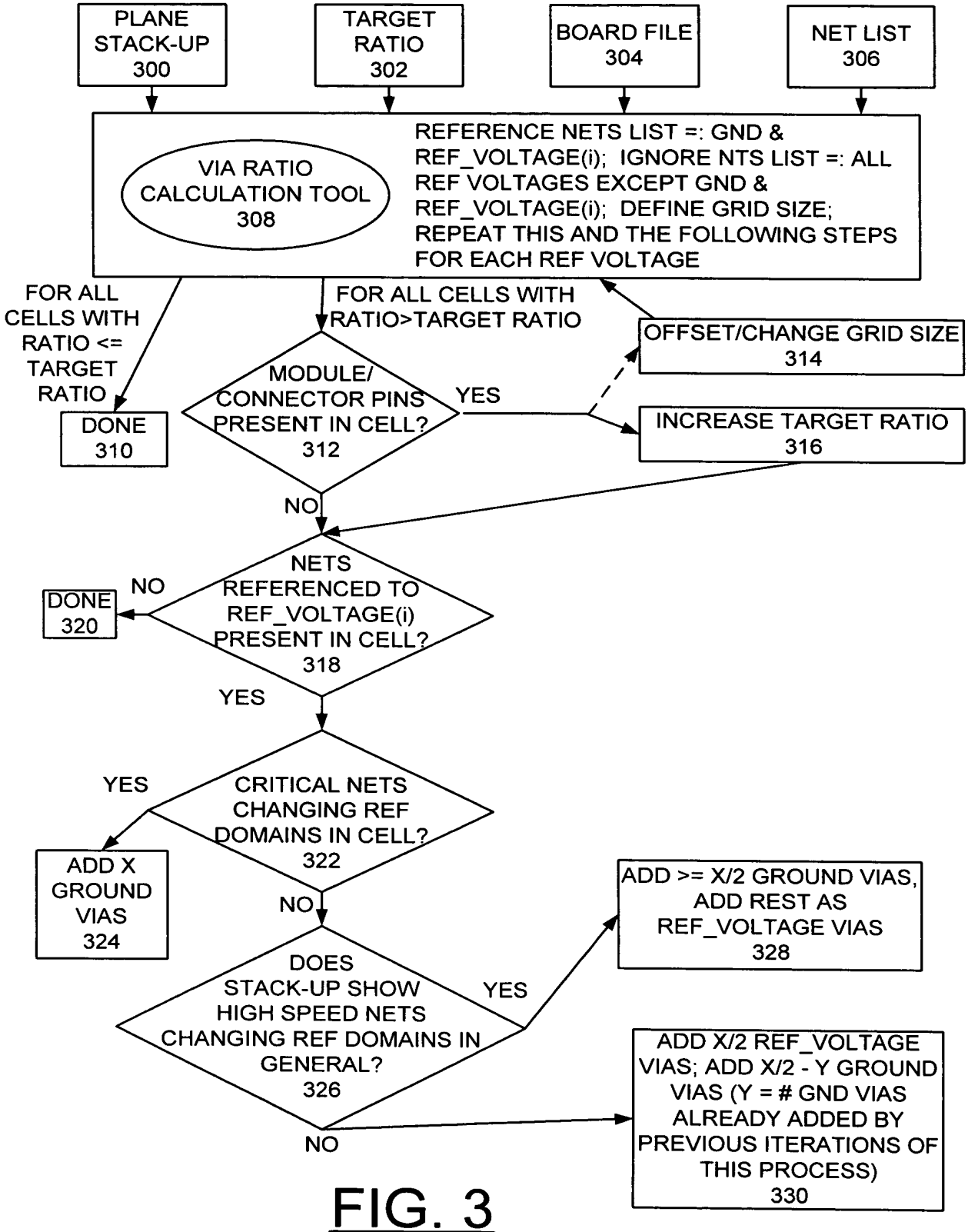

PLANE STACK-UP 300
TARGET RATIO 302
BOARD FILE 304
NET LIST 306
VIA RATIO CALCULATION TOOL 308
REFERENCE NETS LIST =: GND & REF_VOLTAGE(i); IGNORE NTS LIST =: ALL REF VOLTAGES EXCEPT GND & REF_VOLTAGE(i); DEFINE GRID SIZE; REPEAT THIS AND THE FOLLOWING STEPS FOR EACH REF VOLTAGE
FOR ALL CELLS WITH RATIO <= TARGET RATIO
FOR ALL CELLS WITH RATIO>TARGET RATIO
OFFSET/CHANGE GRID SIZE 314
DONE 310
MODULE/ CONNECTOR PINS PRESENT IN CELL? 312
YES
INCREASE TARGET RATIO 316
NO
NETS REFERENCED TO REF_VOLTAGE(i) PRESENT IN CELL? 318
NO
DONE 320
YES
CRITICAL NETS CHANGING REF DOMAINS IN CELL? 322
YES
ADD X GROUND VIAS 324
NO
DOES STACK-UP SHOW HIGH SPEED NETS CHANGING REF DOMAINS IN GENERAL? 326
YES
ADD >= X/2 GROUND VIAS, ADD REST AS REF_VOLTAGE VIAS 328
NO
ADD X/2 REF_VOLTAGE VIAS; ADD X/2 - Y GROUND VIAS (Y = # GND VIAS ALREADY ADDED BY PREVIOUS ITERATIONS OF THIS PROCESS) 330

FIG. 3